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DESIGNING NETWORKS OF SPIKING SILICON NEURONS AND SYNAPSES

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1 INTRODUCTION

Biological neurons communicate with each other via short, fixed-amplitude pulses called *action potentials* or *spikes*. This discrete-amplitude continuous-time representation encodes intensity and timing information with high noise immunity, and thus is ideally suited for processing real-world sensory stimuli.

Since the properties of transistors are well matched to the properties of ionic channels in nerve membranes, Mead has advocated the use of analog VLSI for the construction of artificial neural systems [1]. The current state of the art in realistic single-neuron designs is the silicon neuron of Mahowald and Douglas [2], which exhibits the spiking, refractory, and adaptation characteristics of cortical neurons. The next step in this emerging engineering discipline is the construction of networks of spiking silicon neurons and synapses. This task will require the design and characterization of simple neuron and synapse circuit primitives, and the integrated development of suitable design tools, particularly for schematic capture and simulation.

This paper describes simple and compact silicon neurons and synapses, a neural schematic capture package, and a fast event-driven simulation program optimized for networks of these circuit primitives. The circuits and design tools have been used in the successful design of several small silicon networks.

2 CIRCUIT MODELS

The circuit models are shown in Figure 1. A refractory integrate-and-fire model is the basis for the neuron circuit. The neuron circuit models the behavior of voltage-gated sodium and potassium channels in a simple neuron [3]. An optional tonic current may be injected into the neuron circuit. A simplified synaptic cleft model is the basis for the synapse circuit. A spike from the presynaptic cell causes the release of neurotransmitter into the synaptic cleft, where it remains for a controlled duration. While neurotransmitter is in the cleft, current is injected into the postsynaptic cell. Any number of synapses may be connected to a neuron circuit. Symbols for the neuron, synapse, and tonic input circuits are shown in Figure 2.

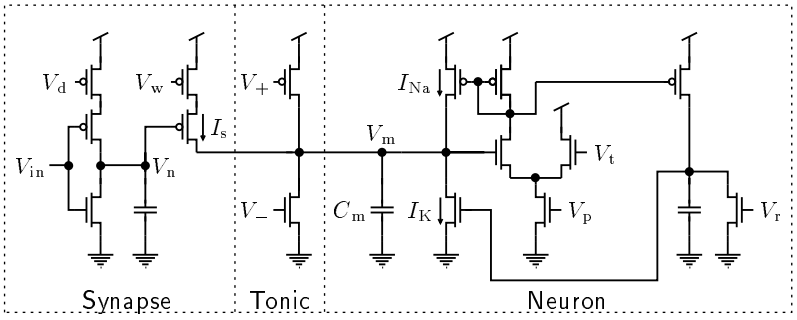

Figure 1 Circuit primitives for the neuron, tonic input, and excitatory synapse. Currents may be injected onto the neuron membrane capacitance C_m by the tonic input and synapse circuits. Within the neuron circuit, the currents I_{Na} and I_K cause action potentials when the membrane voltage V_m reaches the threshold voltage set by V_t. The pulse width and refractory period are controlled by the bias voltages V_p and V_r. The output of the neuron circuit is the membrane voltage V_m. The tonic current is controlled by the bias voltages V_+ and V_-. The input to the synapse circuit is a spike on V_{in}, which results in the appearance of "neurotransmitter", as represented by a low voltage on V_n, for a duration controlled by the bias voltage V_d. The synaptic current I_s is controlled by the weight voltage V_w and gated by V_n. An inhibitory synapse circuit may be made by inverting the direction of current injection with a current mirror.

3 DESIGN TOOLS

The circuits in Figure 1 may be interconnected to form a network of spiking silicon neurons and synapses. However, it is desirable to simulate the operation

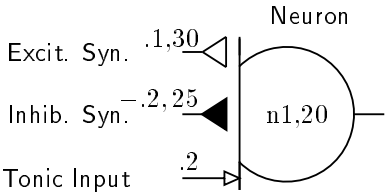

Figure 2 Symbols. The two parameters on the neuron symbol are an identifier label and the refractory period in ms. Default values for the membrane capacitance and threshold voltage are 1 pF and 1 V respectively. The two parameters on the synapse symbol are the synaptic weight current in nA and neurotransmitter duration in ms. The parameter on the tonic input symbol is the tonic input current in nA.

of a network before committing the design to silicon fabrication. A schematic capture program is used to describe the network in a machine-readable format; the correct operation of the network may then be verified via a simulation program.

Neural Schematic Capture

The prototype neural schematic capture package is based on the public-domain program `Analog`, by John Lazzaro and Dave Gillespie. `Analog` allows convenient placement and connection of user-definable symbols, specification of component parameters, and creation of a network description file in `ntk` format. The combination of the program `Analog` and the custom symbol definitions shown in Figure 2 constitutes the neural schematic capture package `Neuralog`.

Neural Simulator

The synapses act like switched constant-current sources onto the membrane capacitance, leading to piecewise-linear membrane voltage trajectories, as shown in Figure 3. A fast event-driven simulation program, called `Spike`, has been written to exploit this behavior. A similar program was written by Pratt [4], but without the schematic capture front-end or the direct link to VLSI circuit primitives. `Spike` maintains a queue of scheduled events; the occurrence of one event usually triggers the scheduling of new events, either immediately or at some later time. The simulation runs until there are no more events in the queue, or until the desired run time has elapsed.

`Spike` reads the `ntk` file generated by `Neuralog`, computes the network response, and outputs the results for plotting by the program `Cview` by Dave Gillespie, or by *Mathematica.*

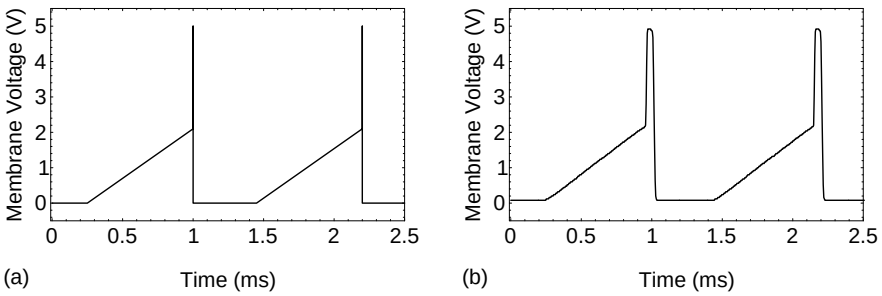

Figure 3 Response of a neuron to an excitatory tonic input. (a) Simulated response. (b) Measured chip response. The neuron integrates the tonic input current, fires an action potential, and remains refractory for a short time before the cycle repeats.

4 EXAMPLE

Central Pattern Generators (CPGs) are groups of neurons that generate rhythmic firing patterns during repetitive motor tasks [5]. A very simple CPG circuit, called a tonic burster, is shown in Figure 4, as an example of a simple network of spiking neurons. Many other networks of spiking neurons have been built and tested, including neural postprocessors for silicon cochleas, and an adaptive spiking network that learns a time delay.

5 CONCLUSIONS

The contribution of the present work is in developing a unified framework of circuit primitives and integrated software tools for neural schematic capture and simulation, to facilitate the investigation of new network designs before committing to silicon fabrication.

6 ACKNOWLEDGMENTS

The author gratefully acknowledges many helpful discussions with Carver Mead, Misha Mahowald, Sylvie Ryckebusch, Rahul Sarpeshkar, and Brad Minch. Special thanks go to John Lazzaro and Dave Gillespie for writing and supporting the Caltech design tools `Analog` and `Cview`. Chip fabrication was provided by DARPA and MOSIS. *Mathematica* is a registered trademark of Wolfram Research, Inc.

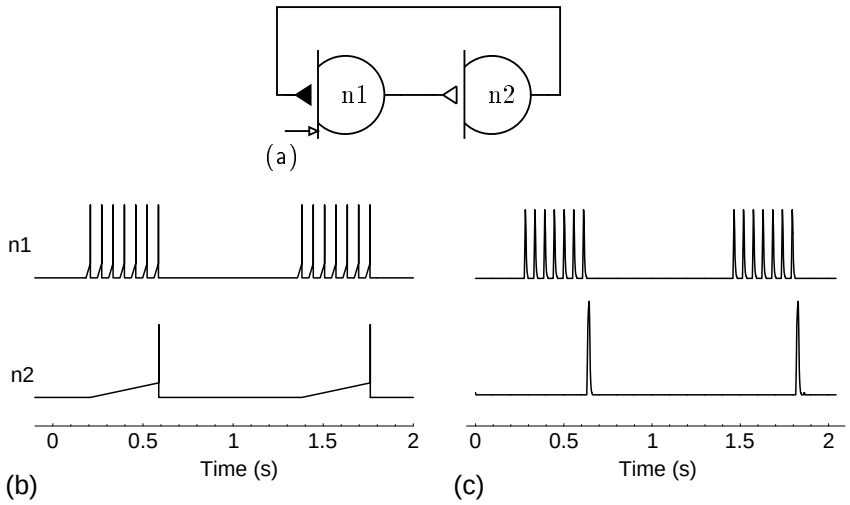

Figure 4 The tonic burster. (a) Schematic diagram. (b) Simulated response. (c) Measured chip response (spikes only). Neuron n1 has an excitatory tonic input that causes it to fire repeatedly. A weakly excitatory synapse couples it to neuron n2, which fires after several spikes from neuron n1. The firing of n2 inhibits n1 for a long time; when the inhibition subsides, n1 begins firing again.

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